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AN 8.0 WATT K-BAND FET AMPLIFIER FOR SATELLITE DOWNLINK

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ABSTRACT

An 8.2 Watt FET amplifier with 38.6 ± 0.5 dB gain over 17.7 to 19.1 GHz frequency band has been developed. This amplifier combines the outputs of eight multistage amplifier modules utilizing a radial combiner. This state-of-the-art power level has been achieved with a noise figure of less than 8.0 dB and AM/PM of less than 2°/dB. The third order intermodulation products at 1 dB gain compression were 20 dBc and variation in group delay over the frequency band was less than ± .25 nSec.

Introduction

The growth of satellite communication traffic indicates that presently allocated C and Ku band spectrum will saturate in the near future. With the recent advances in GaAs power device technology[1] to higher frequencies and with the use of radial combining techniques,[2] it is now possible to have solid state transmitters in K-band. The radial combiner, being less lossy compared to the other binary or serial combiners, provides the most economical combining method to achieve the required high output power.

This paper describes the results achieved by combining 16 power devices. A combination of Lange interdigitated couplers and an 8 way radial combiner has been successfully demonstrated to obtain 8.2 Watts over 17.7 to 19.1 GHz frequency band. An advantage of this combining scheme is the graceful degradation of gain and output power in case one or more device failure. The overall amplifier exhibits excellent phase linearity, low intermodulation products, AM/PM conversion and noise figure performance.

Device Selection and Stage Design

Device selection is the most important criterion for successful completion of any amplifier program. Two special devices were developed by Raytheon for this project. The design consisted of the conventional interdigitated structure, in which many gates are connected in parallel to achieve the required output power. The unit gate width was optimized for high frequency operation and 100μm was selected; the gate length (0.6 to 0.7μm) was chosen to be the shortest consistent with high yield optical lithography. The device design consists of 8 gates combined to form one cell, which yielded 0.5 Watt output power with 5 dB gain. The output device shown in Figure 1 consists of two cells to give 1.0 Watt with 4.5 dB gain. The total gate width of a 2 cell device was 1.6 mm. The via hole technique was employed to minimize the thermal resistance and the source inductance, the two most important parameters for high frequency and high power operation. The integrated plated heat sink, together with extremely thin GaAs chip and via hole processing, ensures minimum thermal resistance.[7] Aluminum was chosen for gate metalization because submicron gates can be readily fabricated with high yield using aluminum.

In designing the single state amplifier, first the device S-parameters were measured up to 18.0 GHz. An accurate model was then derived to extrapolate the device parameters up to 21.0 GHz by computing the model response. Low power driver stages were designed based on the predicted S parameters. The substitution method was employed to get the optimum impedance contours for the high power devices. The large signal characteristics thus obtained were utilized to design the high power output stages.

Module Development

For manufacturing ease, a modular approach was selected to build the transmitter amplifier shown in the block diagram of Figure 2. Two different type modules were used; a driver module with 21 dB gain and 25.5 dBm output power and a power module with 10 dB gain and output power in excess of 31.0 dBm. The block diagram of the power module is shown in Figure 3. The driver module is electrically identical to the power module except it uses lower power devices due to gain and efficiency considerations. All the modules used in this transmitter consist of two cascaded stages driving a higher power balanced stage. These modules were built by utilizing the design techniques explained in the preceeding section. All the components of driver and power modules were built using 15 mil fused silica substrate. The six finger interdigitated coupler used tantalum nitride resistive film to realize the thin film termination resistor. All the modules were assembled and tuned with waveguide to microstrip transition on the input and output. The results obtained from the first two modules cascaded together have already been reported.[4] 1.25 Watts output power with 30 ± 0.5 dB gain was achieved over 17.7 to 19.1 GHz frequency band.

Radial Splitter/Combiner

In order to achieve higher power levels, an 8-way radial splitter/combiner was developed. The splitter and combiner are identical components and are a useful tool for enhancing the output power of an amplifier system beyond the capabilities of an individual device or module.[5] It can combine any number of amplifiers in one stage in contrast to planar binary hybrids such as Wilkinson or Lange couplers.[6] Due to its short interconnecting lines the radial combiner has lower loss and excellent phase and amplitude balance. A computer program was developed to design the microstrip divider to optimize the return loss on all ports, transmission loss and isolation between radial ports by varying the matching circuit, tapered line and the resistor shape. Because of the heat dissipation considerations, the combiner and dividers were fabricated on 25 mil thick BeO. The design provides greater than 20% bandwidth, less than 0.8 dB combining loss and excellent phase and amplitude balance. These detailed results on the combiner developed for this program are reported in a different session.

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Amplifier Performance

The transmitter amplifier with block diagram, shown in Figure 2, was assembled using the amplifier modules and splitter combiner described in the preceeding sections. Figure 11 shows the photograph of the completely assembled unit. Frequency response of the completed transmitter is shown in Figure 4. It covers from 17.7 to 19.1 GHz frequency band with 39.0 dB gain and ± 0.5 dB gain flatness. The transfer characteristic of the transmitter amplifier at 18.4 GHz is shown in Figure 5. It exhibits 8.2 Watts (39.13 dBm) output power at 1 dB gain compression point. It also demonstrates excellent power limiting capability under saturated condition.

The group delay of the amplifier measured from 17.5 to 18.5 GHz is shown in Figure 6. It exhibits a constant group delay of 8.7 nSec with a variation of only 0.25 nSec in 1.0 GHz bandwidth. This is an important parameter in a communication amplifier which indirectly indicates the excellent phase linearity. AM/PM conversion, another important characteristic of the amplifier, was measured over 6.0 dB variation in the input power. The worst variation (2°/dB) was observed at the low drive level. The intermodulation performance was measured at different points in the band with two equal amplitude carriers 50 MHz apart. The photograph of Figure 7 shows the third order intermodulation distortion at 1 dB gain compression point measured at mid band. It was typically 20 dB below either of the two carriers in the complete 1.4 GHz band. The overall transmitter, including all the D.C. power supply and regulators, is shown in the photograph of Figure 8.

Conclusion

State-of-the-art performance has been demonstrated with solid state FET power amplifier in K-band. This amplifier delivers 8.2 Watts of output power with 39.0 dB gain over 1.4 GHz frequency band. The design of this multistage amplifier comprises the power, gain and bandwidth and linearity of the amplifier performance. Power, bandwidth and efficiency of the FET amplifiers can be further improved with improvement in the device technology. With all the devices operating around 110°C junction temperature, the life of the amplifier was better than 10 years based on the device MTFF of 10^7 hours extrapolated from high temperature stress tests. The results achieved here show that GaAs solid state amplifiers are good potential candidates for replacing the TWTA's in the future communication systems.

Acknowledgment

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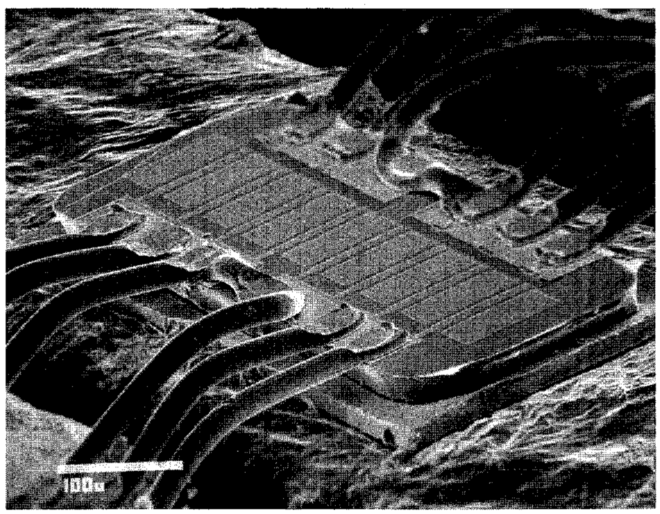

Figure 1. Raytheon 1 W Device

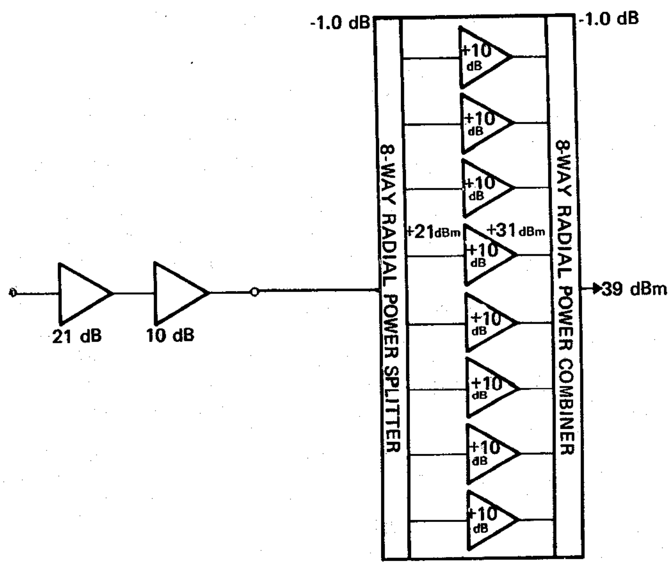

Figure 2. Block Diagram

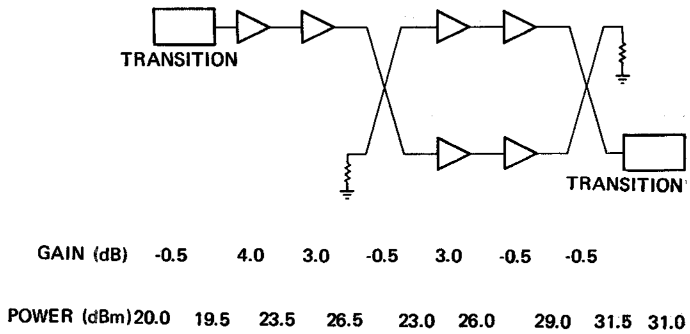

Figure 3. Power Gain Budget of Power Amplifier

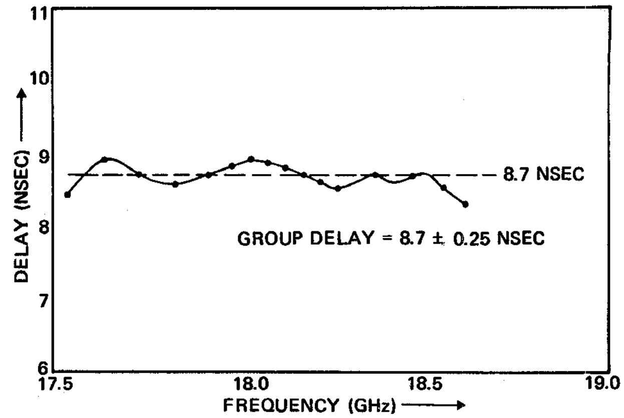

Figure 6. Transmitter Group Delay Response

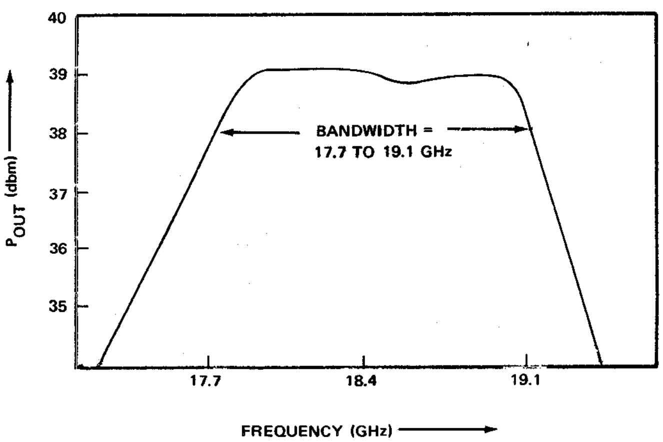

Figure 4. Transmitter Frequency Response

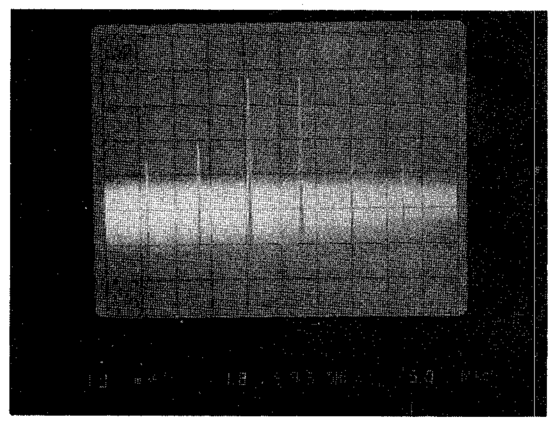

Figure 7. Transmitter Intermodulation Characteristics (Frequency = 18.5 GHz)

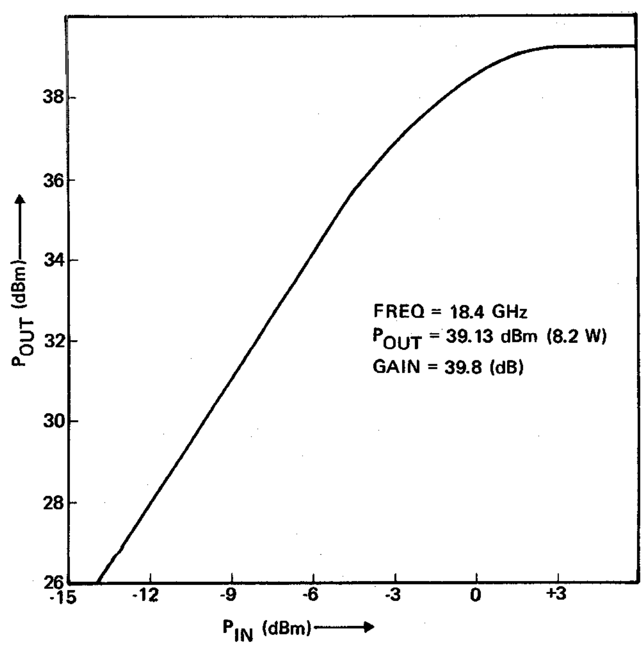

Figure 5. P_{IN}/P_{OUT} Characteristics of Transmitter

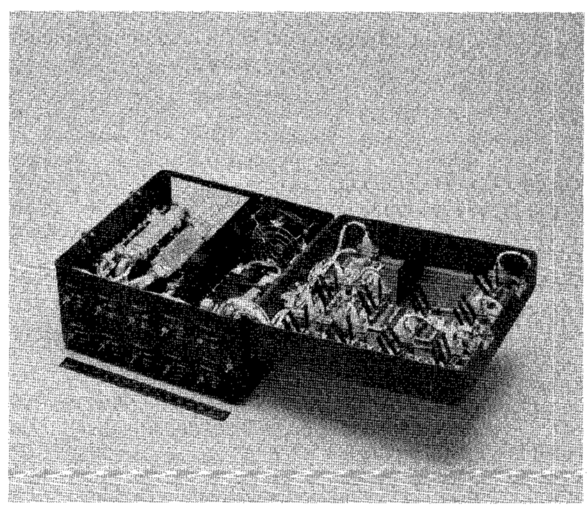

Figure 8. Complete Transmitter Amplifier